Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Applicants cancel claims 73-76.

Listing of Claims:

Claims 1-76 (Canceled)

77. (Previously Presented) A method of transferring data to or from a memory device in either a first operating mode or a second operating mode, the method comprising:

in the first operating mode, transferring data to or from 2N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal; and

in the second operating mode, transferring data to or from N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal.

78. (Previously Presented) The method of claim 77 wherein the acts of transferring data to or from the data bus terminals comprise transferring data from the data bus terminals in a data read operation.

79. (Previously Presented) The method of claim 78 wherein the act of transferring data to or from 2N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

transferring a first set of M*N data bits from a memory array in a first read operation;

storing the read M*N data bits;

transferring a second set of M*N data bits from the memory array in a second read operation; and

sequentially transferring M bits of the stored M*N data bits and the M data bits in the second set of M*N data bits from each of the 2N data bus terminals.

80. (Previously Presented) The method of claim 79 wherein the acts of transferring a first set of M*N data bits from a memory array in a first read operation and transferring a second set of M*N data bits from the memory array in a second read operation comprise transferring M*N bits from the memory array in parallel in each of the first and second read operations.

81. (Previously Presented) The method of claim 78 wherein the act of transferring data to or from N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

transferring a M*N data bits from a memory array in a read operation;

sequentially transferring M bits from each of the N data bus terminals.

82. (Previously Presented) The method of claim 81 wherein the act of transferring M*N data bits from a memory array in a read operation comprises transferring M*N bits from the memory array in parallel during the read operation.

83. (Previously Presented) The method of claim 78 wherein the act of transferring data to or from 2N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

transferring a first set of M/2 parallel data bits from a memory array for each of the 2N data bus terminals;

transferring a second set of M/2 parallel data bits from the memory array for each of the 2N data bus terminals;

converting the transferred first and second sets of M/2 parallel data bits to M serial data bits for each of the 2N data bus terminals; and

coupling the M serial data bits from each of the 2N data bus terminals.

84. (Previously Presented) The method of claim 78 wherein the act of transferring data to or from N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

transferring M parallel data bits from a memory array for each of the N data bus terminals;

converting the transferred M parallel data bits to M serial data bits for each of the N data bus terminals; and

coupling each of the M serial data bits from each of the N data bus terminals.

85. (Previously Presented) The method of claim 77 wherein N is equal to 8 and M is equal to 8.

86. (Previously Presented) The method of claim 77 wherein the acts of transferring data to or from the data bus terminals comprise transferring data to the data bus terminals in a data write operation.

87. (Previously Presented) The method of claim 86 wherein the act of transferring data to or from 2N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

sequentially transferring M bits of data to each of the 2N data bus terminals.

transferring a first set of M*N data bits to a memory array in a first write operation;

transferring a second set of M*N data bits to the memory array in a second write operation.

88. (Previously Presented) The method of claim 87 wherein the acts of transferring a first set of M*N data bits to a memory array in a first write operation and transferring a second set of M*N data bits to the memory array in a second write operation comprise transferring M*N bits to the memory array in parallel in each of the first and second write operations.

89. (Previously Presented) The method of claim 86 wherein the act of transferring data to or from N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

sequentially transferring M bits to each of the N data bus terminals.

transferring a M*N data bits to a memory array in a write operation;

90. (Previously Presented) The method of claim 89 wherein the act of transferring M*N data bits to a memory array in a write operation comprises transferring M*N bits to the memory array in parallel in the write operation.

91. (Previously Presented) The method of claim 86 wherein the act of transferring data to or from 2N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

coupling M serial data bits to each of the 2N data bus terminals;

converting the M serial data bits for each of the 2N data bus terminals to first and second sets of M/2 parallel data bits;

transferring the first set of M/2 parallel data bits to a memory array for each of the 2N data bus terminals; and

transferring the second set of M/2 parallel data bits for each of the 2N data bus terminals to the memory array.

92. (Previously Presented) The method of claim 86 wherein the act of transferring data to or from N data bus terminals of the memory device in form of a burst of M bits of data to or from each terminal comprises:

coupling M serial data bits to each of the N data bus terminals;

converting the transferred M serial data bits to M parallel data bits for each of the N data bus terminals; and

transferring the M parallel data bits for each of the N data bus terminals to a memory array.